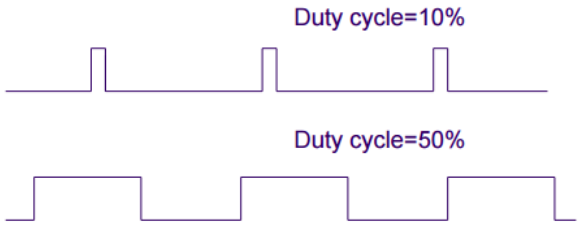
7. Analog I/O

COMP2121 • KC Notes

7.1 Pulse Width Modulation

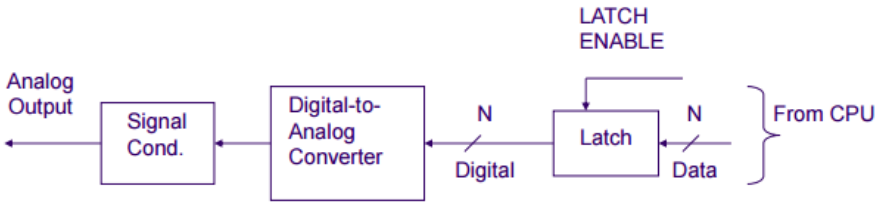
- **Pulse Width Modulation (PWM)**: a way of digitally encoding analog signal levels
  - Relies on **modulating the duty cycle (pulse width/period)** to encode a specific analog signal level
  - Is still digital – either **full high or full low**
  - By changing the **pulse width** of the PWM waveform, we can control the output value



- AVR: timers can be configured for PWM via **TCCR0A**
  - **CTC: clear timer on compare match** – modify the register **TCNTn**, when register value is reached, the counter resets to 0
    - Shorten/lengthen the saw-tooth pulse width
  - **Fast PWM**: when the register value is reached, triggers an update
    - Does not shorten the pulse width, but sets/clears flag
  - **Phase correct PWM**: when register value is reached, triggers an update
    - Is a triangle waveform, similar to Fast PWM

```
ldi temp, 0x4A    ; the value controls the PWM duty cycle
sts OCR5AL, temp
clr temp
sts OCR5AH, temp
                  ; Set the Timer5 to Phase Correct PWM mode.
ldi temp, (1 << CS50)
sts TCCR5B, temp
ldi temp, (1<< WGM50)|(1<COM5A1)
sts TCCR5A, temp
```

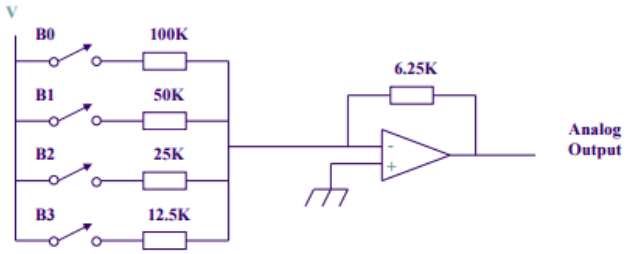
7.2 Digital-to-Analog Conversion



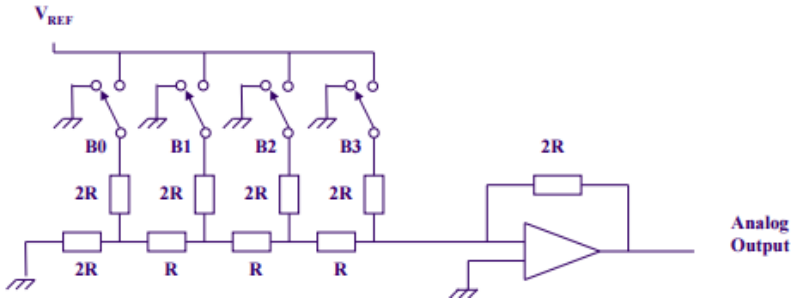
- **Digital to Analog Converter (DAC)**: A **digital value is converted into a continuous value**
  - A **parallel output interface** connects DAC to the CPU
  - Latch may be a part of the DAC or the output interface
  - **Signal condition block** may be used to **filter and smooth** the quantised output, may also perform isolation, buffering, voltage amplification

7.2.1 DAC TYPES

- **Binary-weighted DAC**: A basic DAC circuit that uses **weighted current supplied** to the summing junction of the amplifier (**as switches are closed**)
  - **Higher resolution – more range of resistors**, but temperature and switching problems

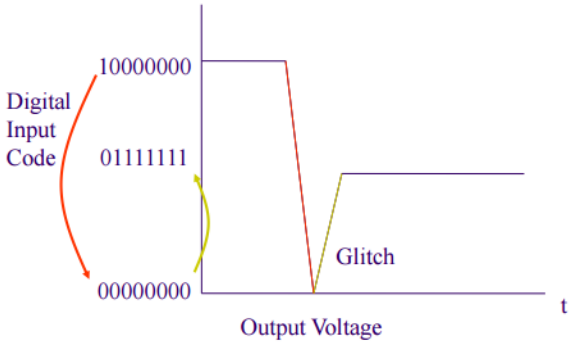


- **R-2R Ladder DAC**: as **switches change from grounded to reference position**, binary weighted current is supplied to summing junction
  - Higher resolution – we only need **more resisters**, not a wide range

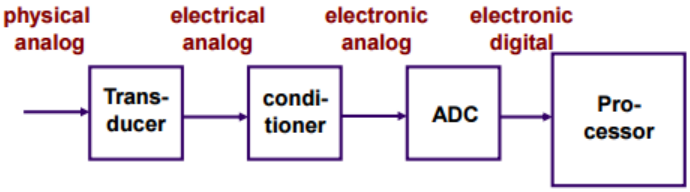


7.2.2 DAC SPECIFICATIONS

- **Resolution and linearity**
  - Resolution determined by the **number of bits** and the output voltage **corresponds to the smallest digital step**, i.e. 1 LSB (least significant bit)
  - Linearity: **deviation in line and the output** (a straight line drawn from zero to full scale, should be around $\frac{1}{2}$LSB)
- **Settling time**: time for the output voltage to settle within an error band, usually $\pm\frac{1}{2}$LSB
- **Glitches**
  - Caused by **asymmetrical switching** in the DAC switches. If the switch changes from 1 to 0 faster than changing 0 to 1 (e.g. 10000000 to 01111111)
  - Can be eliminated using **sample and hold** on the output – sample the data after glitch and settling time



7.3 Analog to Digital Conversion



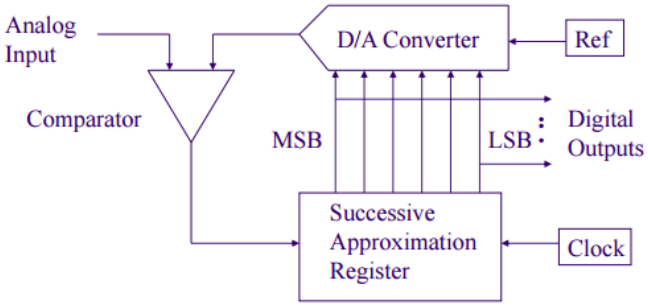
- **Analog to Digital Converter (ADC)**: A **continuous value is converted into a digital value**
  - **Transducer**: converts physical values to electrical signals (voltages or currents)
  - **Signal conditioner**:
    - Electrical **isolation and buffering**: protected from static discharges
    - **Amplification**: produce necessary voltage for the ADC
    - **Bandwidth limiting**: low-pass filter to limit the range of frequencies
  - If several analog inputs are digitised, values are sent to **analog multiplexer**
    - Allows multiple inputs to have its own signal conditioning
    - **Sample-and-hold** circuit holds while ADC converts signals
  - Three-state gates hold digital values generated by ADC

7.3.1 SAMPLING

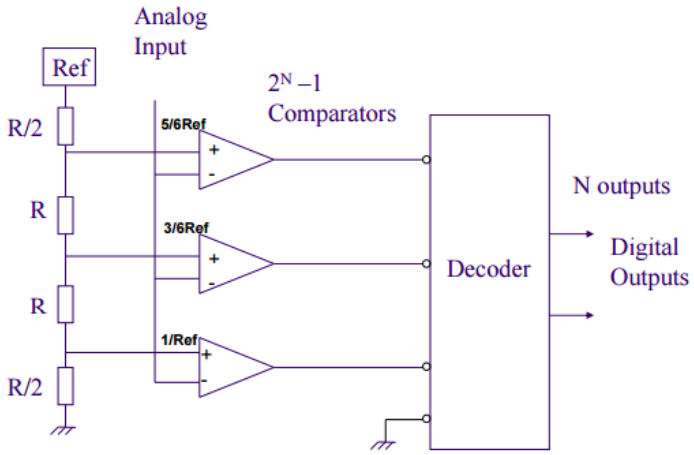
- **Claude Shannon's Sampling Theorem**: the **sampling frequency must be twice the signal frequency** to preserve the full information of the signal
  - Known as the **Nyquist rate**
  - Signal can be exactly reproduced if sample frequency is ≥ Nyquist rate
  - If under, it is considered **undersampled** and will become **aliased** (bad!)

7.3.2 ADC TYPES

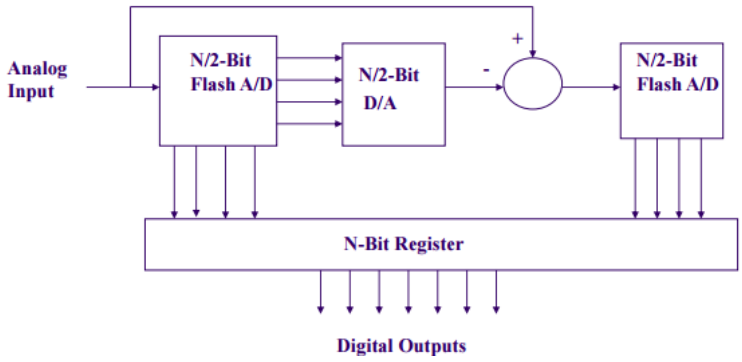
- **Successive Approximation Converter**: Each bit in the approximation register is tested **starting from the most to the least significant bit**
  - As each bit is set, **output of DAC** is compared with the input
  - If D/A output is lower, **bit remains set and next bit is tried**
  - If D/A output is higher, bit is reset
  - **N bit-times** needed to set and test all bits in succession



- **Parallel A/D Converter**: an array of **2^N-1 parallel comparators** that produce output code in **proportional time** of comparators and encoder/decoder logic
  - Fast but more costly
  - Also called flash A/D converter



- **Two-Stage Parallel A/D Converter**: lest costly than parallel (high res, high speed)
  - A **coarse estimate** by the first parallel converter and sent to the summer
  - Subtracted from original, **difference is converted and combined** with first A/D



7.3.3 ADC SPECIFICATIONS

- **Conversion time**: time required to complete a conversion
  - An **upper signal frequency limit t**hat can be sampled without aliasing:
  - E.g. for an ADC with conversion time of 100ms, $f_{max} = 5kHz$

$$f_{max} = \frac{1}{2} f_{sample} = \frac{1}{2 \times \text{conversion time}}$$

- **Resolution**: **Number of bits** in the ADC – which is equivalent to the **smallest input signal for which the ADC will produce a digital code**
  - Usually given as the number of bits, or a percentage of full-scale signal
  - E.g. an 8-bit ADC on 5V full-scale signal, $res = 19.5mV$ or 0.4%

$$\text{Resolution} = \frac{\text{full scale signal}}{2^n}$$

- **Accuracy**: Smallest signal/noise to the measured signal, as a percentage
  - How close the signal is to the actual value

$$\text{Accuracy} = \frac{V_{resolution}}{V_{signal}}$$

- **Linearity**: **deviation in line and the output** (a straight line drawn from zero to full scale, should be around $\frac{1}{2}$ LSB)
- **Missing codes**: internal error in the successive approximation converter
- **Aperture time**: time the ADC is looking at the input signal – change in input signal while it is looking can cause error in output

7.3.4 ADC ERRORS

- **Noise**: reduce noise or choose a resolution to control the peak-to-peak noise
- **Aliasing**: Errors are difficult to quantify and depend on amplitude of signals at frequencies below and above Nyquist frequency
- **Aperture**: A significant error due to **signal variation during aperture time**
  - Uncertainty $\Delta V < 1$ LSB
  - Design equation for aperture time $t_{AP} = \frac{1}{2\pi f_{MAX} 2^n}$