5. AVR Interrupts

COMP2121 • KC Notes

5.1 AVR Interrupts

- Divided into **internal and external interrupts**
  - Each device has a **dedicated interrupt vector**
  - Hardware-recognised interrupts
  - Enable **the enable bit** for the interrupt and the **Global Interrupt Enable (I) bit** (sei)
  - Disable (maskable) bits by resetting the I (cli)
  - Priority of interrupts for multiple interrupts
- Interrupt execution is **five clock cycles**: 2 for saving program counter, 3 for jumping to ISR
- Interrupt has a **32-bit (2-word) interrupt vector** – instruction to be executed after MCU accepts interrupt
  - Defined in the lowest addresses of program memory
  - Priority is based on position of vector in program memory
  - RESET has highest priority

5.1.1 INTERRUPT PROCESS

1. Global Interrupt Enable bit is cleared, **all interrupts disabled** (can be set again for nested interrupts)
2. I bit is set again when **Return from Interrupt instruction RETI** is called
3. AVR exiting an interrupt will return to main program **and execute one more instruction before any other interrupt is served**

5.1.2 RESET

- **Power-on Reset**: when supply voltage is below Power-on Reset threshold VPOT
- **External Reset**: when low level is present on RESET pin for a pulse length
- **Watchdog Reset**: When Watchdog Timer expires and Watchdog is enabled
- **Brown-out Reset**: When VCC is below Brown-out Reset threshold VBOT and Brown-out Detector is enabled
- **JTAG AVR Reset**: When a logic one is in the reset register
- A flag in MCU Control and State Register MCUCSR can be used to determine source of interrupt

5.2 Watchdog Timer

- **Watchdog Timer**: I/O device on the microcontroller that serves as a **counter clocked from a separate on-chip oscillator**
- Controlled to produce different time intervals
- Often used to detect **software crashes** – generates Reset interrupts when its period expires
- Enabled via WDCE bit and WDE bit in the WDTCSR
- Program needs to reset the Watchdog Reset Flag in MCU Control Register MCUCSR before its period expires

Bit	7	6	5	4	3	2	1	0	
(0x60)	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	WDTCSR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	X	0	0	0	

- WDP0-3: prescaler, determines watchdog time reset intervals
- WDE: watchdog enable (enable/disable watchdog)
- WDCE: watchdog change enable (before any changes are made)
- WDIE: watchdog interrupt enable
- WDIF: watchdog interrupt flag

5.3 External Interrupts

- **INT7:0 pins** if enabled (if configured as outputs, you can generate a software interrupt)
- Can be triggered by a **falling or rising edge** via **External Interrupt Control Register**
    - **EICRA for INT3:0, EICRB for INT7:4**
- Enabled via I bit in **SREG** and INTx bit in **EIMSK**
- **EIMSK**: **External Interrupt Mask Register**, 8 bits for each interrupt enable
- **EICRA/B**: **External Interrupt Control Register A/B**, defines **type of signal** on **rising or falling edge**

7	6	5	4	3	2	1	0
ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00

ISCn1	ISCn0	Description
0	0	The low level of INTn generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INTn generates asynchronously an interrupt request.
1	1	The rising edge of INTn generates asynchronously an interrupt request.

- **EIFR**: **Interrupt flag register**, set when an interrupt is enabled and the related INT pin happens (i.e. when the signal edge is activated), 8 bits for each interrupt flag

5.4 Timers/Counters

- Binary counters used as either **timer** (time periods) or **counters** (events or pulse)
- AVR: Timer 0 and 2 are 8 bit, Timer 1, 3, 4, 5 are 16-bit

5.4.1 8-BIT TIMER/COUNTER

- Can be initialised as 0 or a number, counts up or down (direction signal)
- Outputs:
    - **Overflow interrupt request** bit
    - **Output Compare interrupt request** bit
    - **OCn** bit: Output Compare bit for waveform generation
- **TIMSK0**: **Timer/Counter Interrupt Mask Register**, to enable interrupt (and I in SREG)
    - **T0IE0**: enable **overflow interrupt**
    - **OCIE0A/B**: enable **compare match interrupt**
- **TIFR0**: **Timer/Counter Interrupt Flag Register**
    - **OCF0A/B**: bit is set when **compare match** between counter and data in **OCR0A/B**
        - i.e. $(\mathrm{I} = 1)$ && $(\mathrm{OCIE0A/B}) = 1$ && $(\mathrm{OCF0A/B}) = 1$, interrupt is executed and flag is set
        - Bit is cleared by hardware when interrupt is handled, or cleared by writing 0
    - **TOV0**: bit is set when **overflow** occurs in the counter
        - i.e. $(\mathrm{I} = 1)$ && $(\mathrm{TOIE0} = 1)$ && $(\mathrm{TOV0} = 1)$, interrupt is executed and flag is set
        - Bit is similarly cleared when handled or written in
- **TCCR0A/B**: **Timer/Counter Control Register**
    - **COM0xn/WGM0n/FOC0**: control the mode of operation
        - WGM: Waveform Generation mode
        - COM: Compare Output mode
        - Normal mode when WGM02:00 = 00
    - **CS02:00**: clock select bit description – determines the prescaling on the clock
        - E.g. **if prescaler is set to 8, 7812 interrupts per second**
        - $256 \times 8 \div 16\ \mathrm{MHz} = 128\ \mu\mathrm{s}$ where 256 is when it ticks over, 8 is the clock period, 16 is the frequency of the clock
        - $\frac{1\mathrm{s}}{128\mu\mathrm{s}} = 7812/\mathrm{second}$